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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,412	11/16/2001	Nigel G. Herron	X-916 US	3726

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,412	HERRON ET AL.	
	Examiner	Art Unit	
	David Ton	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/20/04 (IDS)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 16-31* is/are allowed.

6)☒ Claim(s) *8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-31 are presented for examination.

Claim Rejections - 35 USC ' 102

2. Claim 8 is rejected under 35 U.S.C. § 102(b) as being clearly anticipated by **Beebe et al.** (Beebe) patent no. **6,021,513**.

3. As to claim 8, Beebe teaches the invention as claimed, including an FPGA comprising:

an FPGA fabric portion [see Fig. 9 and claim 6];

a gasket [programmable interconnects, see claim 6] formed at least partially within the FPGA fabric portion, the gasket forming interfacing logic between an embedded core device [programmable logic units, see claim 6] and the fabric portion; and

isolation circuitry [see claims 8-10] formed within the Gasket, the isolation circuitry being serially coupled to receive test signals from the FPGA portion [see claim 18].

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9-10 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over **Beebe et al.** (Beebe) patent no. **6,021,513**, in view of **Yee** patent no. **5,675,589**.

6. As to claim 9, Beebe does not teach the isolation circuitry includes a multiplexer array for sending test signal directly to a device under test.

Yee teaches a circuit and method for testing FPGA comprises a programmable multiplexer array for sending test signal to the FPGA logic [see Fig. 4B].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Beebe to include the programmable multiplexer array taught by Yee to form an interface for testing selected FPGA logic. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would improve test efficiency and effectiveness.

7. As to claim 10, Yee teaches the multiplexer for sending test signal outputs directly [see "scan out MUX" of Fig. 2].

8. As to claim 11, Beebe teaches the invention substantially as claimed including and FPGA comprising:

an FPGA fabric portion [see Fig. 9 and claim 6];
a gasket [programmable interconnects, see claim 6] formed at least partially within the FPGA fabric portion, the gasket forming interfacing logic between an embedded core device [programmable logic units, see claim 6] and the fabric portion; and a fixed logic device [boundary scan chain, see claim 18] formed within the gasket.

Beebe does not teach the fixed logic device being coupled between a multiplexer and the FPGA fabric portion.

Yee teaches a circuit and method for testing FPGA comprises a programmable multiplexer for connecting the FPGA to one or more scan chains [see Fig. 2 and 4B].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Beebe to include the programmable multiplexer taught by Yee to form an interface for testing selected FPGA logic device. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would improve test efficiency and effectiveness.

9. As to claims 12-15, Yee teaches the multiplexer for receiving outputs from logic device [see "scan out MUX" of Fig. 2].

Allowable Subject Matter

10. Claims 1-7 and 16-31 are allowed.

Conclusion

11. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043.

The examiner can normally be reached on Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DT

September 28, 2004

DAVID TON
PRIMARY EXAMINER